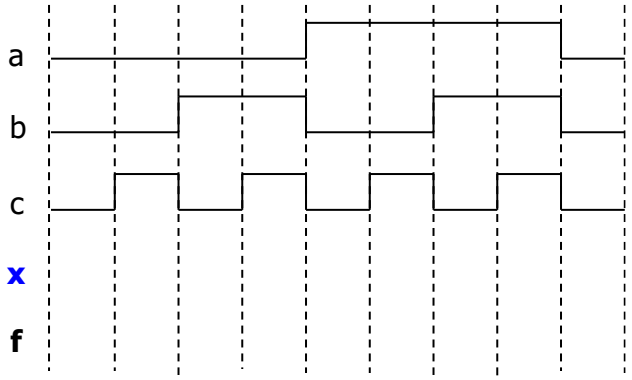
Quiz 1

(September 26th @ 5:30 pm)

PROBLEM 1 (35 PTS)

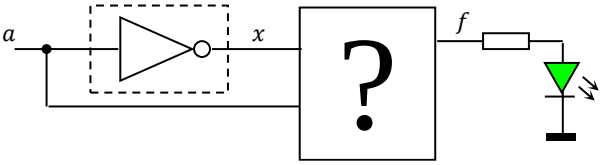
- Complete the timing diagram of the logic circuit whose VHDL description is shown below:

```
library ieee;
use ieee.std_logic_1164.all;

entity test is
  port ( a, b, c: in std_logic;
         f: out std_logic);
end test;

architecture struct of test is
  signal x: std_logic;
begin
  f <= x xnor (not (b));
  x <= a or (not (c));
end struct;
```



PROBLEM 2 (30 PTS)

- Design a circuit that verifies the logical operation of a NOT gate. f='1' (LED ON) if the NOT gate does not work properly. Assumption: when the NOT gate is not working, it generates 1's instead of 0's and vice versa.



PROBLEM 3 (35 PTS)

- The following is the timing diagram of a logic circuit with three inputs. Simplify the Boolean expression of the circuit and sketch the minimized circuit.